

CLAIMS

What is claimed is:

1. An apparatus for exception handling in a data packet processor, comprising:
5 a packet processing pipeline including at least two processing stages for processing a sequential plurality of data packets, each of said plurality of data packets having an exception map associated therewith;
an exception detector associated with each of said processing stages, said detector
10 detecting whether any of a plurality of exception conditions applies to a data packet; and
a bit setter responsive to said exception detector to set, modify, or reset at least one of a plurality of bits of an exception map associated with the data packet.

2. The apparatus of claim 1 wherein each of said exception conditions further
15 comprise a plurality of logical operations.

3. The apparatus of claim 1 further comprising an exception handler to process said exception map in response to said bits that are set in said exception map when all of said processing stages are complete.
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4. The apparatus of claim 1 further comprising a memory associated with said data packet to store said exception map.

5. An apparatus for exception handling in a data packet processor, comprising:
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a packet processing pipeline including at least two processing stages for processing a sequential plurality of data packets, each of said plurality of data packets having an exception map associated therewith;

an exception detector associated with each of said processing stages, said detector
5 detecting whether any of a plurality of exception conditions applies to a data packet;
a bit setter responsive to said exception detector to set, modify, or reset at least one of a plurality of bits of an exception map associated with the data packet; and
an exception handler to further process the data packet in response to said exception map when all of said processing stages are complete.

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6. The apparatus of claim 5 wherein said associated exception condition further comprises a plurality of logical operations.

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7. The apparatus of claim 5 wherein said interpreter further comprises a memory associated with said data packet to store said exception map.

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8. An apparatus for exception handling in a data packet processor, comprising:
means for processing a sequential plurality of data packets through at least one processing stage, each of said plurality of data packets associated with an exception map;
means for detecting whether any of a plurality of exception conditions applies to said data packet in each processing stage; and

means for setting, modifying, or resetting at least one of a plurality of bits in said exception map if it is determined that any of said exception conditions applies to said data packets.

5 9. The apparatus of claim 8 wherein each of said exception conditions further comprise a plurality of logical operations.

10. The apparatus of claim 8 further comprising a means for processing said exception map in response to said bits that are set in said exception map when all of said
10 processing stages are complete.

11. The apparatus of claim 8 further comprising a memory associated with said data packet to store said exception map.

15 12. An apparatus for exception handling in a data packet processor, comprising:
 means for processing a sequential plurality of data packets through at least two processing stages, each of said plurality of data packets having an exception map associated therewith;
20 means for detecting in each of said processing stages whether any of a plurality of exception conditions applies to a data packet;
 means for setting, modifying, or resetting at least one of a plurality of bits of an exception map associated with said data packet; and

means for processing the data packet in response to said exception map when all of said processing stages are complete.

13. The apparatus of claim 12 wherein said associated exception condition further
5 comprises a plurality of logical operations.

14. The apparatus of claim 12 further comprising a means for storing said exception map.

10 15. An apparatus for exception handling in a data packet processor, comprising:
a packet processing pipeline including at least two processing stages for
processing a sequential plurality of data packets, each of said plurality of data packets
having an exception map associated therewith;
an exception detector associated with each of said processing stages, said detector
15 detecting whether any of a plurality of exception conditions applies to a data packet; and
means for setting, modifying, or resetting one or more of a plurality of bits of an
exception map associated with the data packet.

16. The apparatus of claim 15 wherein each of said exception conditions further
20 comprise a plurality of logical operations.

17. The apparatus of claim 15 further comprising a means for processing said exception map in response to said bits that are set in said exception map when all of said processing stages are complete.

5 18. The apparatus of claim 15 further comprising a memory associated with said data packet to store said exception map.

19. An apparatus for exception handling, comprising:
a packet processing pipeline including at least two processing stages for
10 processing a sequential plurality of data packets, each of said plurality of data packets having an exception map associated therewith;
an exception detector associated with each of said processing stages, said detector detecting whether any of a plurality of exception conditions applies to a data packet;
means for setting, modifying, or resetting one or more of a plurality of bits of an
15 exception map associated with the data packet; and
means for processing said exception map in response to said exception map when all of said processing stages are complete.

20. The apparatus of claim 19 wherein each of said exception conditions further
20 comprise a plurality of logical operations.

21. The apparatus of claim 19 further comprising a memory associated with said data packet to store said exception map.

22. A method for exception handling in a data packet processor, comprising:

processing a plurality of data packets through at least two processing stages in
said data packet processor, each of said data packets having an exception map associated
5 therewith;

determining whether any of a plurality of associated exception conditions applies
to a data packet; and

setting, modifying, or resetting one or more a plurality of bits of an exception map
associated with the data packet.

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23. The method of claim 22 further comprising applying logical operations to each of
said plurality of exception conditions.

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24. The method of claim 22 further comprising processing said exception map in
response to said bits that are set in said exception map when all of said processing stages
are complete.

25. The method of claim 22 further comprising storing said exception map in a
memory associated with said data packet.

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26. A method for exception handling in a data packet processor, comprising:

processing a plurality of data packets through at least one processing stage in said data packet processor, each of said data packets having an exception map associated therewith;

determining whether any of a plurality of associated exception conditions applies
5 to a data packet;

setting, modifying, or resetting at least one of a plurality of bits of an exception map associated with the data packet; and

processing said associated data packet in response to said exception map when all of said processing stages are complete.

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27. The method of claim 26 further comprising applying logical operations to each of said plurality of exception conditions.

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28. The method of claim 26 further comprising storing said exception map in a memory associated with said data packet.

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29. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for exception handling in a data packet processor, said method comprising:
processing a plurality of data packets through at least two processing stages in said data packet processor, each of said data packets having an exception map associated therewith;

determining whether any of a plurality of associated exception conditions applies to a data packet; and

setting, modifying, or resetting one or more a plurality of bits of an exception map associated with the data packet.

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30. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for exception handling in a data packet processor, said method comprising:

processing a plurality of data packets through at least one processing stage in said data packet processor, each of said data packets having an exception map associated therewith;

determining whether any of a plurality of associated exception conditions applies to a data packet;

setting, modifying, or resetting at least one of a plurality of bits of an exception map associated with the data packet; and

processing said associated data packet in response to said exception map when all of said processing stages are complete.

31. An apparatus for exception handling in a data packet processor, comprising:
means for processing a plurality of data packets through at least two processing stages in said data packet processor, each of said data packets having an exception map associated therewith;

means for determining whether any of a plurality of associated exception conditions applies to a data packet; and

means for setting, modifying, or resetting one or more a plurality of bits of an exception map associated with the data packet.

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32. The apparatus of claim 31 further comprising means for applying logical operations to each of said plurality of exception conditions.

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33. The apparatus of claim 31 further comprising means for processing said exception map in response to said bits that are set in said exception map when all of said processing stages are complete.

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34. The apparatus of claim 31 further comprising means for storing said exception map in a memory associated with said data packet.

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35. An apparatus for exception handling in a data packet processor, comprising:
means for processing a plurality of data packets through at least one processing stage in said data packet processor, each of said data packets having an exception map associated therewith;

means for determining whether any of a plurality of associated exception conditions applies to a data packet;

means for setting, modifying, or resetting at least one of a plurality of bits of an exception map associated with the data packet; and

means for processing said associated data packet in response to said exception map when all of said processing stages are complete.

36. The method of claim 35 further comprising means for applying logical operations
5 to each of said plurality of exception conditions.

37. The method of claim 35 further comprising means for storing said exception map in a memory associated with said data packet.

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